IN THE CLAIMS

Please cancel claims 1-12 without prejudice or disclaimer, and add new claims 13-22 as follows:

1–12. (Cancel)

13. (New) A high frequency power amplifier circuit, comprising:

a plurality of amplifying stages which are coupled in cascade between an input terminal and an output terminal for amplification, each of the amplifying stage including a field effect transistor as an amplifier;

a bias circuit which supplies bias voltages set to predetermined values to control terminals of the plurality of amplifying stages; and

a power source voltage control circuit which is coupled between a power source voltage and the amplifying stages, receives the power source voltage, and generates a first power voltage for a final one of said amplifying stages, said final amplifying stage being nearest to the output terminal and generates a second power voltage for preceding ones of said amplifying stages in accordance with an output power specification signal,

wherein the power source voltage control circuit includes a first control transistor for controlling the first power voltage and a second control transistor which is different form the first control transistor for controlling the second power voltage, and

wherein the power source voltage control circuit set the second power voltages to determine a current flow on said preceding amplifying stages in a saturate state, when the first power voltage is set to determine a current flow on the final stage in a liner state.

14. (New) A high frequency power amplifier circuit according to claim 13, wherein the power source voltage control circuit further includes a first differential circuit which receives the output power specification signal and the first power voltage and supplies a first control voltage to the first control transistor, and a second differential circuit which receives the output power specification signal and the second power voltage and supplies a second control voltage to the second control transistor.

15. (New) A high frequency power amplifier circuit, comprising:

a first amplifying stage having a first amplifier transistor which receives an input signal to be amplified and a power source voltage, and a first control transistor which receives an output power specification signal and is connected the first amplifying stage in series;

a second amplifying stage having a second amplifier transistor which receives an output of the first amplifying stage and the power source voltage, and a second control transistor which receives the output power specification signal;

a third amplifying stage having a third amplifier transistor which receives an output of the second amplifying stage and outputs an output signal amplified by the third amplifying stage;

a bias circuit which supplies bias voltages set to predetermined values to input terminals of the first, second and third amplifying stages; and

a power source voltage control circuit which is coupled between the power source voltage and the third amplifying stage, receives the power source voltage, and generates a power voltage for the third amplifying stage in accordance with an output power specification signal,

wherein the power source voltage control circuit includes a power source control transistor for controlling the first power voltage, and

wherein the power source voltage control circuit set the power voltages to determine a current flow on the third stage in a liner state, when a current flow on the first and the second amplifying stages in a saturate state.

16. (New) A high frequency power amplifier circuit according to claim 15,

wherein the first amplifier transistor and the first control transistor form a first dual gate field effect transistor, and

wherein the second amplifier transistor and the second control transistor form a second dual gate field effect transistor.

17. (New) A high frequency power amplifier circuit according to claim 16, wherein the power source voltage control circuit further includes a differential circuit which receives the output power specification signal and the power voltage, and supplies a control voltage to the power source control transistor .

18. (New) A high frequency power amplifier circuit according to claim 13,

wherein date widths of the field effect transistors as amplifiers included in the amplifying stages increase in order from one of the amplifying stages nearest to the input terminal to the final amplifying stage such that the current flows on said preceding amplifying stages in a saturate state, when the current flows on the final stage in a liner state

19. (New) A high frequency power amplifier circuit according to claim 15,

wherein date widths of the field effect transistors as amplifiers included in the amplifying stages increase in order from the first amplifier stage, the second amplifier stage, to the third amplifier stage for the current flows on the first and the second amplifying stages in a saturate state, when the current flows on the third stage in a liner state.

20. (New) A high frequency power amplifier circuit according to claim 13,

wherein the bias voltages increase in order from one of the amplifying stages nearest to the input terminal to the final amplifying stage such that the current flows on the preceding amplifying stages in a saturate state, when the current flows on the final stage in a liner state.

21. (New) A high frequency power amplifier circuit according to claim 15,

wherein the bias voltage increase in order from the first amplifier stage, the second amplifier stage, to the third amplifier stage for the current flows on the first and the second amplifying stages in a saturate state, when the current flows on the third stage in a liner state.

22. (New) A radio communication system comprising:

a first high frequency power amplifier circuit for amplifying a first frequency band;

a second high frequency power amplifier circuit for amplifying a second frequency band;

a baseband circuit which converts an audio signal into a baseband signal to be transmitted and converts a received signal into an audio signal;

a power source voltage control circuit which is coupled between the power source voltage and the third amplifying stage, receives the power source voltage, and generates a power voltage for the third amplifying stage of the first high frequency power amplifier circuit and for the third amplifying stage of the second high frequency power amplifier circuit in accordance with an output power specification signal; and

a modulation/demodulation circuit which demodulates the received signal and modulates the baseband signal,

wherein each of the first and second high frequency power amplifier circuits includes a first amplifying stage having a first amplifier transistor which receives an input signal to be amplified and a power source voltage, and a first control transistor which receives an output power specification signal and is connected the first amplifying stage in series; a second amplifying stage having a second amplifier transistor which receives an output of the first amplifying stage and the power source voltage, and a second control transistor which receives the output power specification signal; a third amplifying stage having a third amplifier transistor which receives an output of the second amplifying stage and outputs an output signal amplified by the third amplifying stage; a bias circuit which supplies bias voltages set to predetermined values to input terminals of the first, second and third amplifying stages; and a power source voltage control circuit which is coupled between the power source voltage and the third amplifying stage, receives the power source voltage, and generates a power voltage for the third amplifying stage in accordance with an output power specification signal, the power source voltage control circuit includes a power source control transistor for controlling the first power voltage, and the power source voltage control circuit set the power voltages to determine a current flow on the third stage in a liner state, when a current flow on the first and the second amplifying stages in a saturate state,

wherein the first high frequency power amplifier circuit amplifies the baseband signal and outputs a first transmission signal of the first frequency band,

wherein the second high frequency power amplifier circuit amplifies the baseband signal and outputs a second transmission signal of the second frequency band, and

wherein a power source control transistor for controlling the first power voltage is included in the power source voltage control circuit and arranged in

common for the third amplifying stages of the first and second high frequency power amplifier circuits.